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09/779,096	02/08/2001	Shi-Tron Lin	B-4101 618582-4	5687

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/779,096	Applicant(s) LIN ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35 and 37-39* is/are pending in the application.

4a) Of the above claim(s) *5-7,11,12,15-30,32 and 33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-10,13,14,31,34,35 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1-4, 8-10, 13-14, 31 and 39 are objected to because of the following informalities: The phrase "a first circuit coupled between a first power line and a pad; and a second circuit coupled between a second power line and the pad, comprising", as recited in claims 1, 2, 31 and 39, is unclear as to whether the term "comprising" refers to the first circuit, the second circuit, or both circuits.

2. Claims 8-9 are objected to because of the following informalities: It is unclear whether the doped region, as recited in claim 1, is the same element as the fourth doped region, as recited in dependent claim 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 34, 35, 37 and 39 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. Figure 2 depicts a DC connection VDD to the first node and the pad. There is no support in the specification for a device which comprises no DC connection to the first node, and no DC connection between the first doped region and the pad, as recited in claims 34 and 39, respectively.

6. There is no support in the specification for a device which comprises a first doped region capacitively coupled to the pad and electrically floated in the well (that is, having no external electrical connections) and has no DC connection between the first doped region and the pad, as recited in claim 39.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 34, 35, 37 and 39 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. The phrase "electrically floated" means that the doped region of the first conductivity type has no external electrical connections. Claim 39 recite a capacitively coupled between a pad and the doped region of the first conductivity type. It is unclear how the doped region of the first conductivity type can be electrically floated in a well and at the same time be connected to a capacitor, as recited in claim 39.

10. The claimed limitations of "the third doped region has no DC connection to the first node", and "there is no DC connection between the first doped region and the pad", as recited in claims 34 and 39, respectively, are unclear as to what is meant by a DC connection between two elements, since DC connection is the coupling of an element to a power source.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 34-35 and 37, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Ham (5,903,420) or Avery (5,343,053).

Ham does not state whether the conductivity type of the substrate is an N type or P type. Both situations will be examined. Assume the substrate has an N conductivity type. Ham teaches in figure 6 and related text (column 3, line 57 to column 4, line 41) an electrostatic discharge protection circuit coupled between a first node Vss arid a second node Vdd, comprising a substrate 20 of a first conductive type; a first doped region 48 and a second doped region 50 of a second conductive type formed in the substrate, the first and second doped regions being spaced apart enabling a channel region (under gate 27b) formed in between; a well region 22 of the second conductive type formed in the substrate; and a third doped region 46 of the first conductive type (note that the third doped region 46 can be an N or P conductive type (column 4, line 17)), electrically floated in the well region, so that the third doped region has no DC connection to the first node, wherein the first node Vss is electrically coupled to the first doped region 48 and the second node Vdd is electrically coupled to the second doped region 50, wherein during an ESD event, the first doped region is coupled to the first end, and wherein the substrate is coupled to the second power line through a sixth doped region.

Regarding the claimed limitation of a first doped region and a second doped region of a second conductive type formed in the substrate, doped regions 48 and 50 are formed in well 24, which in turn is formed in the substrate. Therefore, doped regions 48 and 50 are formed in the substrate, as claimed.

Assume that the substrate has a P conductivity type. Ham teaches in figure 6 and related text (column 3, line 57 to column 4, line 41) an electrostatic discharge protection circuit coupled between a first node Vdd arid a second node Vss, comprising a substrate 20 of a first conductive type; a first doped region 44 and a second doped region 42 of a second conductive type formed in the substrate, the first and second doped regions being spaced apart enabling a channel region (under gate 27a) formed in between; a well region 24 of the second conductive type formed in the substrate; and a third doped region 46 of the first conductive type (note that the third doped region 46 can be an N or P conductive type (column 4, line 17)), electrically floated in the well region, so that the third doped region has no DC connection to the first node, wherein the first node Vdd is electrically coupled to the first doped region 44 and the second node Vss is electrically coupled to the second doped region 42, wherein during an ESD event, the first doped region is coupled to the first end, and wherein the substrate is coupled to the second power line through a sixth doped region.

Regarding the claimed limitation of a first doped region and a second doped region of a second conductive type formed in the substrate, doped regions 44 and 42 are formed in well 22, which in turn is formed in the substrate. Therefore, doped regions 44 and 42 are formed in the substrate, as claimed.

Although Ham does not state that third doped region 46 is electrically floated, the third doped region 46 is not directly connected to any external connections, thus rendering it electrically floated.

Avery teaches in figure 9 and related text a second circuit coupled between a second power line 45 and the pad 47 (see figure 13), comprising: a resistor constructed by a well region 434 of a second conductivity type deposited on a substrate 430 of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region 440 of the second conductivity type (fifth region) at least partially overlapping the well region and coupled to the pad; and a second end of a fifth doped region 448, a first doped region 436 of the first conductivity type deposited between the fourth and fifth doped regions, electrically floated in the well region and having no DC connection to a first node; and an electrostatic discharge protection component 442, 444 coupled between the second end 448 and the second power line 45

Regarding 35, Ham teaches in figure 6 the first node Vss is coupled to the first doped region 48 through the well region 22 (the first situation), and the first node Vdd is coupled to the first doped region 44 through the well region 24 (the second situation).

Regarding 37, although Ham does not state that well regions 22 and 24, respectively, form a resistor element, well regions 22 and 24 form a resistor element because the current flowing in the well regions must have certain resistivity (see also figure 4 and column 2, lines 13-18).

13. Claim 38 is rejected under 35 U.S.C. 102(b) as being anticipated by Wu (5,686,751).

Wu teaches in figures 5 and 6 and related text an ESD protection circuit coupled between a first node and a second node, comprising: a first conductivity type substrate 200, a first doped region and a second doped region 225 of a second conductivity type formed in the substrate 200, the first and second doped regions being spaced apart enabling a channel region formed in between, a well region 220 of the second conductivity type formed in the substrate, and a third doped region 223 of the first conductivity type deposited in the well region; and is coupled to the first node through a capacitor C2, wherein the first node is electrically coupled to the first doped region and the well region, and the second node is electrically coupled to the second doped region 225.

Wu teaches a first doped region and a second doped region of a second conductivity type formed in the substrate, because the broad recitation of the claim does not preclude the first doped region and the second doped region to be formed in a well which in turn is formed in the substrate. Therefore, Wu teaches a first doped region and a second doped region of a second conductivity type formed in the substrate, as claimed.

Wu teaches a first node being electrically coupled to the first doped region and the well region, and a second node being electrically coupled to the second doped region 225, because in an electronic circuit the elements are electrically coupled to each other.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1, 3-4, 8, 13-14, 31, 34-35, 37 and 39, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ham (5,903,420) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 1, 31 and 39, Ham teaches substantially the entire claimed structure, as applied to claim 34 above, including an ESD protection element being a MOSFET comprising a gate a drain coupled to the second end and a source coupled to the power line, wherein during an ESD event, the first doped region is coupled to the first end, and wherein the substrate is coupled to the second power line through a sixth doped region.

Ham does not teach using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad.

AAPA teaches in figure 1 using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Ham's device as a second circuit in an output buffer which

comprises first and second circuits coupled between first and second power lines and a pad in order to use the device in an application which requires an output buffer. Note that it is conventional to use in an output buffer, and the device would not operate without first and second power lines. Furthermore, the recitation of an output buffer which comprises first and second circuits coupled between first and second power lines and a pad occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Moreover, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 39, the claimed limitations of a first doped region capacitively coupled to the pad is inherent in Ham's device, because capacitance exists between the power lines such that the first doped region is capacitively coupled to the pad, as claimed.

16. Claims 1, 8-9, 13-14, 31, 34-35, 37 and 39, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Avery (5,343,053) in view of Applicant Admitted Prior Art (AAPA).

Avery teaches in figure 9 and related text a second circuit coupled between a second power line 45 and the pad 47 (see figure 13), comprising: a resistor constructed by a well region 434 of a second conductivity type deposited on a substrate 430 of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region 440 of the second conductivity type (fifth region) at least partially overlapping the well region and coupled to the pad; and a second end of a fifth doped region 448, a first doped region 436 of the first conductivity type deposited between the fourth and fifth doped regions, electrically floated in the well region and having no DC connection to a first node; and an electrostatic discharge protection component 442, 444 coupled between the second end 448 and the second power line 45, wherein during an ESD event, the first doped region is coupled to the first end, and wherein the substrate is coupled to the second power line through a sixth doped region 446.

Avery does not teach using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad.

AAPA teaches in figure 1 using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Avery's device as a second circuit in an output buffer which

comprises first and second circuits coupled between first and second power lines and a pad in order to use the device in an application which requires an output buffer. Note that it is conventional to use in an output buffer, and the device would not operate without first and second power lines. Furthermore, the recitation of an output buffer which comprises first and second circuits coupled between first and second power lines and a pad occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Moreover, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 39, the claimed limitations of a first doped region capacitively coupled to the pad is inherent in Avery's device, because capacitance exists between the power lines 404 and 406 (see figure 13) such that the first doped region is capacitively coupled to the pad, as claimed.

17. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (5,686,751) in view of Applicant Admitted Prior Art (AAPA).

Wu teaches in figures 5 and 6 and related text a second circuit coupled between a second power line Vdd and a pad 8 (see figure 5), comprising: a resistor constructed by a well region 220 of a second conductivity type deposited on a substrate 200 of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region 225 of the second conductivity type at least partially overlapping the well region and coupled to the pad, a first doped region 223 of the first conductivity type deposited in the well region; a capacitor C2 coupled between the pad and the first doped region 223 (see figure 5), and an electrostatic discharge protection component coupled between the second end and the second power line.

Wu does not teach using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad.

AAPA teaches in figure 1 using the device in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Wu's device as a second circuit in an output buffer which comprises first and second circuits coupled between first and second power lines and a pad in order to use the device in an application which requires an output buffer. Note that it is conventional to use in an output buffer, and the device would not operate without first and second power lines. Furthermore, the recitation of an output buffer

which comprises first and second circuits coupled between first and second power lines and a pad occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Moreover, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Response to Arguments

18. Applicant's arguments with respect to claims 1-4, 8-10, 13-14, 31, 34-35 and 37-39 have been considered but are moot in view of the new ground(s) of rejection.

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-C are cited as being related to ESD devices.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
June 18, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800